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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/069,054	04/28/1998	KING W. CHAN	ACT-233	2978

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EXAMINER	
THOMPSON, ANNETTE M	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/069,054	CHAN ET AL.	
	Examiner	Art Unit	
	A. M. Thompson	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2006 and 28 April 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 1, 2006 has been entered.

2. Applicants' amendment to 09/069,054 has been examined. Claims 4-6, 24-26 are amended. Claims 1-39 are pending.

3. Applicants' amendment has been considered but is not persuasive. The applicable rejections from the prior office action are incorporated herein.

Drawings

4. The replacement drawings sheets for Figures 1-3 were received on June 1, 2006. These drawings are approved.

5. The drawings are objected to because they are poor quality and difficult to discern. Please also not the attached PTO-948. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the

appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

6. Claim 1 is objected to because of the following informalities: Pursuant to claim 1, at line 4, after "blocks", insert a semicolon (;). Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Rejection of claims 1-3, 7-9 and 11-19

8. **Claims 1-3, 7-9 and 11-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Tavana et al., U.S. Patent 5,825,202 (hereinafter "Tavana).** Tavana discloses an integrated circuit with field programmable and application specific logic areas and the interconnections used.

9. Pursuant to claim 1, which recites an interface architecture in an integrated circuit (Tavana, Fig. 2, the interconnect cells; Figs. 3 and 6, cell A; Fig. 5, cell C; Fig. 4, cell B; col. 2, ll. 14-18), comprising an FPGA portion of said integrated circuit having logic blocks for implementing logic functions (Fig. 3, #22, the CLBs) and interconnect conductors for programmably connecting said logic blocks (Fig. 3, #26, the switch matrices and Fig. 3, #s 28 and #24, the PIP, programmable interconnect points); an ASIC portion of said integrated circuit (Fig. 2, #14, ASLA) having mask programmed logic circuits and mask programmed interconnect conductors between said logic circuits (col. 5, ll. 55-64 discloses a mask-defined ASLA; see also col. 5, line 62 reference USP 5,068,604 at Fig. 2, 114a, 114b and '604, col. 10, ll. 9-15); and masked programmed dedicated interface tracks (Fig. 6, #61, 62) connected between said logic blocks in said FPGA portion (Fig. 7, #s 63-66, col. 6, ll. 44-52) and said mask programmed interconnect conductors in said ASIC portion (col. 6, ll. 59-64; see also Fig. 6, #18 and Fig. 7b).

10. Pursuant to claim 2, wherein the interconnect conductors in the FPGA portion include local routing resources: (Tavana discloses that local routing resources are included through the use of switch matrices, col. 5, ll. 31-54; see also Fig. 3).

11. Pursuant to claim 3, wherein interface buffers are disposed in series with said dedicated interface tracks between FPGA portions and ASIC portion (Tavana discloses the option of interconnection using buffer at col. 6, ll. 52-64, Fig. 7b).

12. Pursuant to claim 7, which further includes an FPGA-ASIC routing channel: (Tavana, Fig. 2, col. 5, ll. 13-21).

13. Pursuant to claim 8, wherein the FPGA-ASIC routing channel is mask-programmable: (Tavana, Figs. 3-5, where the routing channel is field configurable and mask programmable, col. 6, ll. 7-27; col. 7, ll. 6-13).

14. Pursuant to claim 9, wherein the FPGA-ASIC routing channel is field-programmable: See Tavana, Figs. 3-5 where the routing channel is field configurable and mask programmable, col. 6, ll. 7-27; col. 7, ll. 6-13.

15. Pursuant to claims 11 and 14, which further includes a plurality of IO modules arranged on the perimeter of the IC: Tavana, Fig. 2, illustrates this limitation; see also col. 4, line 62 to col. 5, line 12.

16. Pursuant to claim 12, wherein one or more of said IO modules are connected to said FPGA portion: Tavana, Fig. 2, col. 4, line 62 to col. 5, line 2.

17. Pursuant to claim 13, wherein one or more of said IO modules are connected to said ASIC portion: Tavana, Fig. 2, col. 4, line 62 to col. 5, line 2.

18. Pursuant to claim 15, wherein one or more of said IO modules are connected to said FPGA-ASIC routing channel: Tavana, Figs. 4 and 5 illustrates this limitations, also see col. 6,, ll. 18-64.

19. Pursuant to claim 16, wherein the ASIC portion is adjacent to one side of said FPGA portion: This limitation is illustrated by Tavana, Figure 2.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Rejection of claims 17-19

22. **Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana.** Tavana discloses all the limitations of claim 1, from which these claims depend but Tavana does not explicitly discloses the exact configuration relating to the placing of the ASIC portion with respect to the FPGA portion. However, Tavana discloses at least one side of the ASIC adjacent to the FPGA. It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to exercise

their design prerogative and modify the design architecture of Tavana to facilitate a routing or timing objective by making the ASIC portion adjacent to two, three or four sides of the FPGA portion.

Rejection of claims 4-6

23. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana as applied to claim 1, supra, in view of Bertolet et al., U.S. Patent 5,671,432 ("Bertolet"). Tavana discloses all the limitations of claim 1 from which claims 4-6 depends. Tavana fails to discloses the specific logic used for the discloses programmable I/O blocks. Bertolet discloses a programmable array having programmable logic cells, a programmable interconnect network and a programmable system. Bertolet teaches an advance I/O system capable of handling high logic densities peculiar to FPGA. It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the teaching of Tavana with Bertolet to provide advanced circuitry for Tavana's dense combined FPGA/ASLA integrated circuit. (The citations reference Bertolet, unless otherwise stated).

24. Pursuant to claim 4, wherein the interface architecture includes an input buffer: Fig. 4, 60a and 60b; an output buffer said output buffer connected to said input buffer: Fig. 4, 58a, 58b; three multiplexers, two of said muxes connected to said output buffer and one of said muxes connected to said input buffer: Fig. 4, 52a, 54a, 56a, 52b, 54b, 56b; a configurable register, said configurable register connected to each of said muxes: Bertolet, Fig. 6, details the muxes illustrated in Fig. 4. Bertolet Fig. 6, shows memory elements connected to each mux. Bertolet further teaches that the memory

contains user programming information which is the same as configuration information, col. 8, ll. 2-16.

25. Pursuant to claim 5, wherein the interface architecture includes an input buffer: Fig. 4, 60a and 60b; an output buffer said output buffer connected to said input buffer: Fig. 4, 58a, 58b; three multiplexers, two of said muxes connected to said output buffer and one of said muxes connected to said input buffer: Fig. 4, 52a, 54a, 56a, 52b, 54b, 56b; a memory store, said memory store connected to each of said muxes, Bertolet, Fig. 6, details the muxes illustrated in Figure 4. Bertolet Fig. 6, shows memory elements connected to each mux. Bertolet further teaches that the memory contains user programming information which is the same as configuration information, col. 8, ll. 2-16.

26. Pursuant to claim 6, wherein the interface architecture includes an input buffer: Fig. 4, 60a and 60b; an output buffer said output buffer connected to said input buffer: Fig. 4, 58a, 58b; three multiplexers, two of said muxes connected to said output buffer and one of said muxes connected to said input buffer: Fig. 4, 52a, 54a, 56a, 52b, 54b, 56b; programmable elements, said programmable elements connected to each of said muxes: Bertolet, Fig. 6, details the muxes illustrated in Figure 4. Bertolet Fig. 6, shows memory elements connected to each mux; see also Bertolet, col. 8, ll. 2-16 which teaches that the memory contains user programming information.

Rejection of claim 10

27. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana as applied to claim 1, supra, in view of Sharma et al., U.S. Patent 5,878,051 ("Sharma").

28. Tavana discloses all the limitations of the claim from which claim 10 depends. However, Tavana does not disclose the inclusion of JTAG buffers between the FPGA and the ASIC logic portions. Sharma discloses an FPGA which is reconfigured during a test mode to perform testing of an ASIC or other IC component, col. 2, ll. 18-61. It would have been obvious to one of ordinary skill in the art to modify the teaching of Tavana with Sharma and use the IEEE JTAG standard to provide interface ports between the ASIC and the FPGA to enable testing of the FPGA-ASIC assemblage.

29. Pursuant to claim 10, wherein there are JTAG buffers arranged between said dedicated interface tracks and ASIC portions: Sharma, Fig. 2, col. 5, ll. 8-56; see also col. 8, ll. 4-65.

Rejection of claims 16-19

30. Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana in view of Applicant's admitted prior art.

31. Tavana discloses all the limitations of claim 1, from which claims 16-19 depends but does not discloses the exact configurations relating to the placing of the ASIC portion with respect to the FPGA portion. Applicants' admitted prior art (AAPA) discloses these limitations and it would have been obvious to one of ordinary skill in the

art to rely on, consider, and incorporate what is already well known prior art in determining further improvements.

32. Pursuant to claim 16 wherein said ASIC portion is adjacent to one side of said FPGA portion: AAPA, Fig. 1A, 1B.

33. Pursuant to claim 17 wherein said ASIC portion is adjacent to two sides of said FPGA portion: AAPA, Fig. 1C, 1D.

34. Pursuant to claim 18 wherein said ASIC portion is adjacent to three sides of said FPGA portion: AAPA, Fig. 1C, 1D (including the side between the I/O and the FPGA and ASIC.

35. Pursuant to claim 19 wherein said ASIC portion is adjacent to four sides of said FPGA portion: AAPA, Fig. 1E, 1F.

Rejection of claim 20

36. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana in view of the Aggarwal et al paper and Rush, U.S. patent 5,742,181.

37. Tavana discloses all the limitations of claim 1 from which claim 20 depends, but fails to discloses hierarchical design structures. The Aggarwal paper discloses routing architectures for hierarchical field programmable gate arrays. Rush discloses FPGAs with hierarchical interconnect structures. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify Tavana with the Aggarwal paper and Rush and implement a hierarchical FPGA having the advantages of lower density and increased routing efficiency.

38. Pursuant to claim 20, wherein the FPGA portion has a hierarchical design: The Aggarwal paper teaches FPGA hierarchical designs, pages 475-477. Rush teaches FPGAs or generally programmable atomic logic elements with a hierarchical interconnect structure, col. 4, line 10 to col. 13, line 8.

Rejection of claims 21-23, 27-29, 31-36

39. **Claims 21-23, 27-29, 31-36 are rejected under 35 USC 103(a) as being unpatentable over Tavana in view of the Aggarwal paper and Rush.** Tavana discloses an integrated circuit with filed programmable and application specific logic areas (ASLA) and the interconnections. Tavana does not teach hierarchical design structures. The Aggarwal paper discloses routing architectures for hierarchical field programmable gate arrays. Rush discloses FPGAs with hierarchical interconnect structures. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify Tavana with the Aggarwal paper and Rush and implement a hierarchical FPGA having the advantages of lower density and increased routing efficiency.

40. Pursuant to claim 21 which recites an interface architecture in an integrated circuit, (Tavana, Figs. 3-5 discloses interface architecture that is either mask-defined or FPGA programmable), comprising an FPGA portion of said integrated circuit having a plurality of levels, each of said levels containing local routing resources and a plurality of blocks, each of said blocks including either a module or another of said levels (Tavana, col. 2, ll. 4-9, col. 5, ll. 31-54); an ASIC portion of said integrated circuit having mask programmed interconnect conductors between logic portions of said ASIC portion

(Tavana discloses a mask-defined ASLA, col. 5, ll. 55-64); masked programmed dedicated interface tracks (Fig. 6, #61, 62) connected between said modules or blocks in said FPGA portion (Fig. 7, #s 63-66, col. 6, ll. 44-52) and said mask programmed interconnect conductors in said ASIC portion (col. 6, ll. 59-64; see also Fig. 6, #18 and Fig. 7b).

41. Pursuant to claim 22, wherein each of said blocks in said FPGA portion contains local routing resources (Tavana discloses that local routing resources are included through the use of switch matrices, col. 5, ll. 31-54; see also Fig. 3).

42. Pursuant to claim 23, wherein interface buffers are arranged between said dedicated interface tracks and said ASIC portion (Tavana discloses the option of interconnection using buffer at col. 6, ll. 34-64).

43. Pursuant to claim 27, which further includes an FPGA-ASIC routing channel arranged between said dedicated interface tracks and said ASIC portion (Tavana, Fig. 2, col. 5, ll. 13-21).

44. Pursuant to claim 28, wherein the FPGA-ASIC routing channel is mask-programmable: (See Tavana, Figs. 3-5, where the routing channel is field configurable and mask programmable, col. 6, ll. 7-27; col. 7, ll. 6-13)

45. Pursuant to claim 29, wherein the FPGA-ASIC routing channel is field-programmable (See Tavana, Figs. 3-5 where the routing channel is field configurable and mask programmable, col. 6, ll. 7-27; col. 7, ll. 6-13).

46. Pursuant to claims 31 and 34, which further includes a plurality of IO modules arranged on the perimeter of the IC: Tavana, Fig. 2, illustrates this limitation; see also col. 4, line 62 to col. 5, line 12.

47. Pursuant to claim 32, wherein one or more of said IO modules are connected to said FPGA portion: Tavana, Fig. 2, col. 4, line 62 to col. 5, line 2.

48. Pursuant to claim 33, wherein one or more of said IO modules are connected to said ASIC portion: Tavana, Fig. 2, col. 4, line 62 to col. 5, line 2.

49. Pursuant to claim 35, wherein one or more of said IO modules are connected to said FPGA-ASIC routing channel: Tavana, Figs. 4 and 5 illustrates this limitations, also see col. 6,, ll. 18-64.

50. Pursuant to claim 36, wherein the ASIC portion is adjacent to one side of said FPGA portion: This limitation is illustrated by Tavana, Figure 2.

Rejection of claims 24-26

51. **Claims 24-26 are rejected under 35 USC 103(a) as being unpatentable over Tavana in view of the Aggarwal paper and Rush as applied to claim 21, supra, and further in view of Bertolet.**

52. Tavana in view of the Aggarwal paper and Rush discloses all the limitations of claim 21 but fails to disclose a programmable array. Bertolet discloses a programmable array having programmable logic cells, a programmable interconnect network and a programmable system. Bertolet teaches an advance I/O system capable of handling high logic densities peculiar to FPGA. It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the teaching of

Tavana, Aggarwal and Rush with Bertolet to provide advanced circuitry for Tavana's dense combined FPGA/ASLA integrated circuit. (The citations reference Bertolet, unless otherwise stated)

53. Pursuant to claim 24, wherein the interface architecture includes an input buffer: Fig. 4, 60a and 60b; an output buffer said output buffer connected to said input buffer: Fig. 4, 58a, 58b; three multiplexors, two of said muxes connected to said output buffer and one of said muxes connected to said input buffer: Fig. 4, 52a, 54a, 56a, 52b, 54b, 56b; a configurable register, said configurable register connected to each of said muxes: Bertolet, Fig. 6, details the muxes illustrated in Fig. 4. Bertolet Fig. 6, shows memory elements connected to each mux. Bertolet further teaches that the memory contains user programming information which is the same as configuration information, col. 8, ll. 2-16.

54. Pursuant to claim 25, wherein the interface architecture includes an input buffer: Fig. 4, 60a and 60b; an output buffer said output buffer connected to said input buffer: Fig. 4, 58a, 58b; three multiplexors, two of said muxes connected to said output buffer and one of said muxes connected to said input buffer: Fig. 4, 52a, 54a, 56a, 52b, 54b, 56b; a memory store, said memory store connected to each of said muxes, Bertolet, Fig. 6, details the muxes illustrated in Figure 4. Bertolet Fig. 6, shows memory elements connected to each mux. Bertolet further teaches that the memory contains user programming information which is the same as configuration information, col. 8, ll. 2-16.

55. Pursuant to claim 26, wherein the interface architecture includes an input buffer: Fig. 4, 60a and 60b; an output buffer said output buffer connected to said input buffer: Fig. 4, 58a, 58b; three multiplexors, two of said muxes connected to said output buffer and one of said muxes connected to said input buffer: Fig. 4, 52a, 54a, 56a, 52b, 54b, 56b; programmable elements, said programmable elements connected to each of said muxes: Bertolet, Fig. 6, details the muxes illustrated in Figure 4. Bertolet Fig. 6, shows memory elements connected to each mux; see also Bertolet, col. 8, ll. 2-16 which teaches that the memory contains user programming information.

Rejection of claim 30

56. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana in view of the Aggarwal paper and Rush as applied to claim 21, supra, and further in view of Sharma. Tavana in view of Aggarwal paper and Rush teaches the limitations of claim 21 from which this claim depends but does not disclose the inclusion of JTAG buffers between the FPGA and AASIC logic portions. Sharma discloses an FPGA which is reconfigured during a test mode to perform testing of an ASIC or other IC component, col. 2, ll. 18-61. It would have been obvious to one of ordinary skill in the art to modify the teachings of Tavana, the Aggarwal paper and Rush with Sharma and use the IEEE JTAG standard to provide interface ports between the ASIC and the FPGA to enable testing of the FPGA-ASIC assemblage.

57. Pursuant to claim 30, wherein there are JTAG buffers arranged between said dedicated interface tracks and ASIC portions: Sharma, Fig. 2, col. 5, ll. 8-56; see also col. 8, ll. 4-65.

Rejection of claims 36-39

58. Claims 36-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana in view of the Aggarwal paper and Rush as applied to claim 21 above and further in view of Applicant's admitted prior art (AAPA) .

59. Tavana in view of the Aggarwal paper and Rush discloses all the limitations of claim 21, from which claims 36-39 depends but does not discloses the exact configurations relating to the placing of the ASIC portion with respect to the FPGA portion. Applicants' admitted prior art (AAPA) discloses these limitations and it would have been obvious to one of ordinary skill in the art to rely on, consider, and incorporate what is already well known prior art in determining further improvements.

60. Pursuant to claim 36 wherein said ASIC portion is adjacent to one side of said FPGA portion: AAPA, Fig. 1A, 1B.

61. Pursuant to claim 37 wherein said ASIC portion is adjacent to two sides of said FPGA portion: AAPA, Fig. 1C, 1D.

62. Pursuant to claim 38 wherein said ASIC portion is adjacent to three sides of said FPGA portion: AAPA, Fig. 1C, 1D (including the side between the I/O and the FPGA and ASIC.

63. Pursuant to claim 39 wherein said ASIC portion is adjacent to four sides of said FPGA portion: AAPA, Fig. 1E, 1F.

Remarks

64. Applicant's primary arguments asserts that Tavana does not disclose or suggest specific claim language recited in independent claims 1 and 21. Specifically,

this claim language recites (at claim 1, lines 7-9) "mask programmed dedicated interface tracks connected between said logic blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion" and (at claim 21, lines 7-9) "mask programmed dedicated interface tracks connected between said modules or blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion". Further to this assertion, Applicants request "that the Examiner point out the specific places in the reference [Tavana] containing such disclosure".

65. Turning first to Tavana's Figure 6, the switch matrices (#26) provide interconnection between the CLBs (#22) (configurable logic blocks) that comprise the FPGA (col. 5, ll. 32-54). Figure 6 discloses special mask-defined lines (#61, #62) that extend across the FPGA and connect to the local interconnect lines of the FPGA (Fig. 7, #s 63-66) that connect to the CLB blocks. It is these special mask-defined lines that are considered as reading on Applicants' limitation of "mask programmed dedicated interface tracks". Further, these special mask-defined lines (#s 61, 62) extend across the FPGA portion of the device (Fig. 6, #12) and connect to the mask programmed interconnect conductors (Fig. 6, #18) of the ASIC portion (#14).

66. Tavana's Figure 3 does not disclose Applicants' disputed limitation, but reads on other sections of Applicants' claimed recitations.

Conclusion

67. Any inquiry concerning this communication or earlier communications should be directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m..

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

68. Responses to this action should be mailed to the appropriate mail stop:

Mail Stop _____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to:

(571) 273-8300, (for all **OFFICIAL** communications intended for entry)

A. M. THOMPSON
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